PCB Layout and Design Guide for CH7513

1.0 INTRODUCTION

Chrontel's CH7513 is an eDP/DP receiver that integrates LVDS Transmitter for the notebook/AIO display. The CH7513 is designed to comply with the DisplayPort (DP) Specification version 1.2 and the Embedded DisplayPort Specification version 1.4. The CH7513 provides support for two main link lanes with data rate running at either 1.62Gb/s or 2.7Gb/s, and accepts data in 18-bit 6:6:6 or 24-bit 8:8:8 RGB digital format. During system power-up, setting the power on/off sequence for a particular panel can be achieved through the Boot ROM registers. The CH7513 has incorporated a brightness control function to interface with LCD backlight module. Brightness control commands sent through AUX Channel are dynamically translated by the CH7513 and converted into the LCD backlight control signals.

The CH7513 can support 18-bit Single Port, 18-bit Dual Port, 24-bit Single Port and 24-bit Dual Port LVDS outputs in both OpenLDI and SPWG bit mapping for LVDS application. The CH7513 supports LVDS output up to 1920x1200.

The CH7513 can be configured as DisplayPort to eDP bypass converter, the 2 lane main link reuses LVDS Tx pins, AUX CH and HPD pass through CH7513 pins. The CH7513 supports 2 Main Link Lanes at either 1.62Gb/s or 2.7Gb/s or 5.4Gb/s link rate for eDP bypass.

This application note focuses only on the basic PCB layout and design guidelines for the CH7513 DP Receiver with LVDS Transmitter. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures presented in this document are based on the 68-pin QFN (8x8 mm) package of the CH7513. Please refer to the CH7513 datasheet for details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7513 should be placed as close as possible to the respective pins. The following will describe guidelines on how to connect critical pins, as well as the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimal power supply decoupling is accomplished by placing a 0.1μF ceramic capacitor at each of the power supply pins as shown in **Figure 1**. These capacitors (C1, C3, C4, C6, C7, C9, C10, C12, C14 and C15) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7513 ground pins, in addition to ground vias.

2.1.1 Ground Pins

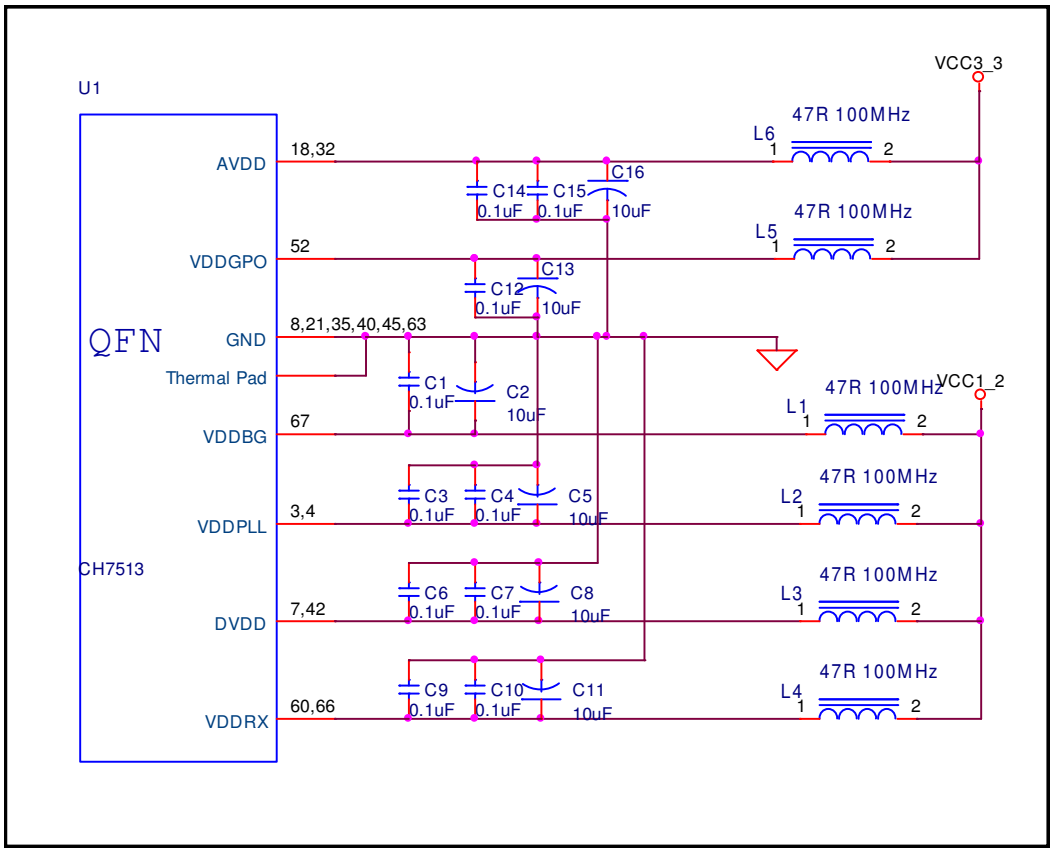
The CH7513 should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7513 ground pins should be connected to its respective decoupling capacitor ground lead directly, and then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 1** for the Ground pin assignments.

2.1.2 Power Supply Pins

There are eleven power supply pins: VDDPLL, DVDD, AVDD, VDDGPO, VDDRX and VDDBG. Refer to **Table 1** for the Power supply pin assignments. Refer to **Figure 1** for Power Supply Decoupling.

Table 1: Power Supply Pin Assignments for the CH7513 (68QFN)

Pin	# of Pins	Type	Symbol	Description
3,4	2	Power	VDDPLL	Stream PLL Power Supply (1.2V)
7,42	2	Power	DVDD	Digital Power Supply (1.2V)
18,32	2	Power	AVDD	LVDS Power Supply (3.3V)
52	1	Power	VDDGPO	GPIO Power Supply (3.3V)
60,66	2	Power	VDDRX	DP Rx Power Supply(1.2V)
67	1	Power	VDDBG	Band-gap Power Supply (1.2V)
8,21,35,40,45,63, Thermal pad	6	Ground	GND	Power ground



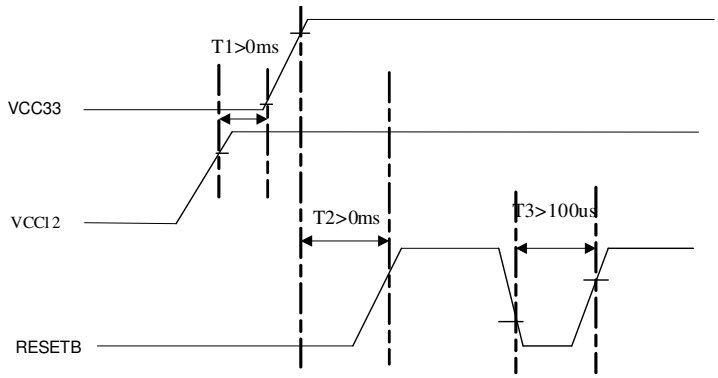


Figure 1: Power Supply Decoupling and Distribution

Note:

1. **The rising time (10%~90%) of power supply should not exceed 2.5ms.**
2. **The power sequence of VCC12 and VCC33 will not affect the normal functionality. To avoid unexpected glitch on LVDS TX pins during power on, the time from VCC12 up to 90% to VCC33 up to 10%, should be greater than 0ms.**
3. **The power supply should be valid (up to 90%) and stable before RESETB becomes invalid.**
4. **The rising threshold of RESETB is DVDD*0.8. The falling threshold of RESETB is DVDD*0.2.**
5. **The pulse width of valid RESETB signal should be at least 100us.**
6. **The exposed pad, which is the thermal pad, must be linked to GND.**
7. **All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05Ω at DC; 23Ω at 25MHz & 47Ωat 100MHz. Refer to Fair Rite part #2743019447 for details (an equivalent part can be used for the diagram).**

2.1.3 Power On and Reset

RESETB pin is the chip reset pin for the CH7513. The CH7513 will be reset when this pin is low. The RESETB pin can be pulled high from 1.2V to 3.3V with a 10K resistor. A reset switch can be placed on the RESETB pin on the PCB as hardware reset for CH7513 as shown in **Figure 3**.

There are two reset methods. One is RC reset. The power supply should be valid and stable before RESETB becomes invalid as shown in **Figure 1**. A 10KΩ and 0.1uF RC reset circuit is recommended.
Another method is using an external reset signal. In this case, the power supply should be valid and stable before the reset signal is valid. The pulse width of valid reset signal should be at least 100us. The timing is shown in **Figure 1.**

2.2 Internal Reference Pins

• RBIAS pin

This pin sets the Band-gap Bias Voltage. A 1 KΩ, 1% tolerance resistor should be connected between RBIAS and GND as shown in **Figure 2**. A smaller resistance will create less Band-gap Bias voltage. The distance between the resistor and the CH7513 should be less than 6mm, the shorter and wider trace the better. For optimal performance, this signal should not overlay the analog power or analog output signals.

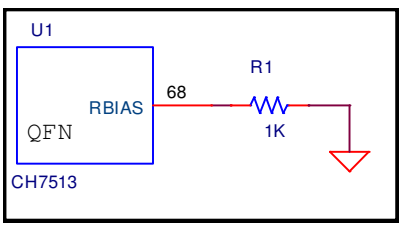


Figure 2: RBIAS Pin Connection

2.3 General Control Pins

• XI, XO

A 27MHz crystal (±30ppm) can be connected to XI and XO as the CH7513 reference clock input. In PCB design, a 27MHz crystal must be placed as close as possible to the XI and XO pins, with traces connected from point to point, overlaying the ground plane. Since the crystal generates the timing reference for the CH7513, it is essential that noise not couple into these input pins.

The crystal load capacitance, CL, is usually specified in the crystal spec from the vendor. Refer to **Figure 3** for a crystal circuit reference design and an example of load capacitors.

• Reference Crystal Oscillator

CH7513 includes an oscillator circuit that allows a predefined-frequency crystal to be connected directly. Alternatively, an externally generated clock source may be supplied to CH7513. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI pin, and the XO pin should be left open. The external source must exhibit ±100 ppm or better frequency accuracy, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be predefined-frequency, ±100 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to CH7513 (C_{ext}).

To be able to tune, a variable capacitor may be connected from XI to ground.

Note that the XI and XO pins each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI and XO pins, the following calculation should be used:

$\mathbf{C}_{ext} = (2 \times C_L) - C_{int} - 2C_S$

Where
C_{ext} = external load capacitance required on XI and XO pins.
C_L = crystal load capacitance specified by crystal manufacturer.
C_{int} = capacitance internal to CH7513 (approximately 10-15 pF on each of XI and XO pins).
C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

In general,
$C_{int}XI = C_{int}XO = C_{int}$
$C_{ext}XI = C_{ext}XO = C_{ext}$

such that $C_L = (C_{int} + C_{ext}) / 2 + C_S$ and $C_{ext} = 2 (C_L - C_S) - C_{int} = 2C_L - (2C_S + C_{int})$

Therefore C_L must be specified greater than $C_{int}/2 + C_S$ in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For detail considerations of crystal oscillator design, please refer to **AN-06**.

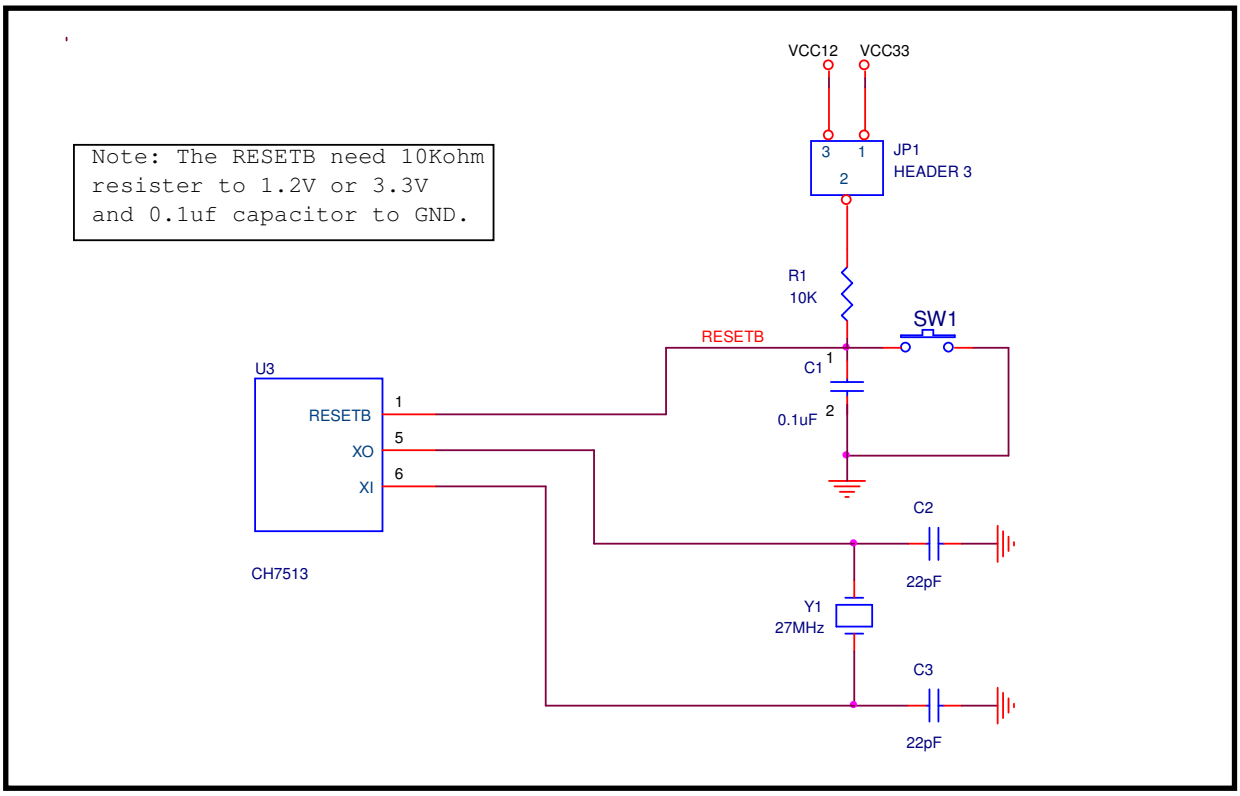


Figure 3: General Control Pins

2.4 Serial Port Control Pins

• SPC0, SPD0 and AS

SPD0 and SPC0 function as a serial interface where SPD0 is the bi-directional data and SPC0 is an input-only serial clock. In the reference design, SPD0 and SPC0 pins are pulled up to +3.3V with 6.8k resistors. Through these two pins, the internal register values of the chip can be read. The external Boot ROM can be updated if these pins are connected to SPC1 and SPD1 with jumpers as shown in **Figure 4**.
AS pin is I2C address selection pin. CH7513 I2C device address is 7'h21 when AS pin is pull high and 7'h23 when AS pin is pull low. A 10K pull-high resistor is used to set default I2C address.

• SPC1 and SPD1

SPD1 and SPC1 function as a serial interface where SPD1 is bi-directional data and SPC1 is an input only serial clock. In the reference design, SPD1 and SPC1 pins are pulled up to +3.3V with 6.8kΩ resistors as shown in **Figure 4**.

SPD1 and SPC1 are used to interface with the CH9905/ CH9904 (the serial Boot ROM). The CH7513 will auto-load the values, such as EDIDs and configurations, etc. , from the Boot ROM upon power-on or reset.

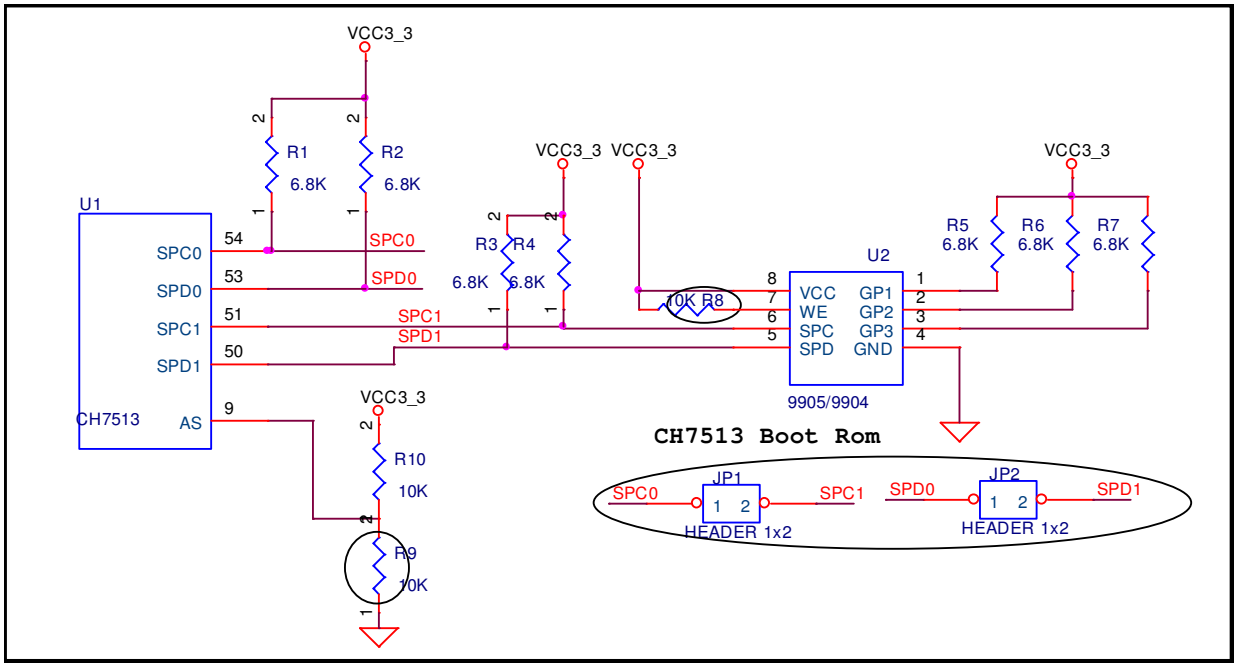


Figure 4: Serial Port Control

Note: If you use SPC0/SPD0 or the AUX channel to update the CH9905/ CH9904 Boot ROM, the precondition is that the MCU firmware must work properly. It is recommended that the IIC/SMBUS be used to update CH9905/ CH9904, by linking the IIC/SMBUS to SPC0 and SPD0

2.5 Display Port Signal Pins

• DP0P/N, DP1P/N

These pins accept two AC-coupled differential pair signals from the Display Port transmitter.
Since the digital serial data of the CH7513 may be toggled at speeds up to 2.7 GHz, it is strongly recommended that the connection of these video signals between the graphics controller and the CH7513 be kept as short as possible, avoid discontinuities in the reference plane and be isolated as much as possible from the analog outputs and analog circuitry. For optimal performance, these signals should not overlay the analog power or analog output signals. When a signal pair has to changes layers, the ground stitching vias should be placed close to the signal vias. A minimum of 1 to 3 stitching vias per pair of signals is recommended. Never route a trace so that it straddles a plane split. It is recommended that 5 mils traces be used in routing these signals. There should be 7 mils spacing between each intra pair. The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 2 inches. Bend smaller than 45 degrees should be avoided. The AC coupling capacitors for the serial video inputs must be placed close to the GMCH, as shown in **Figure 5**.

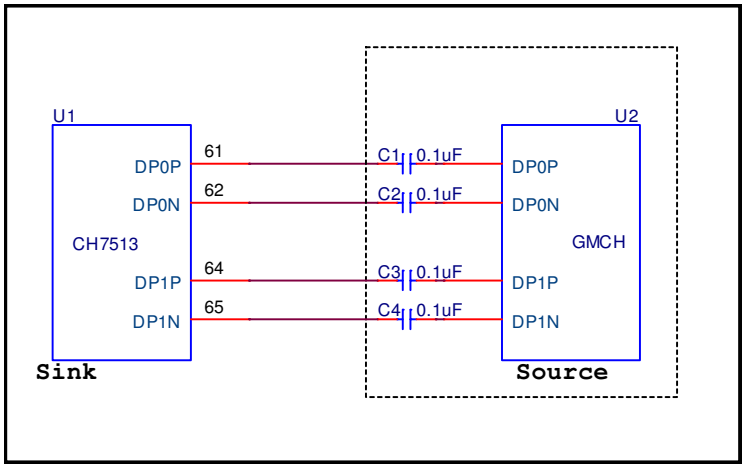


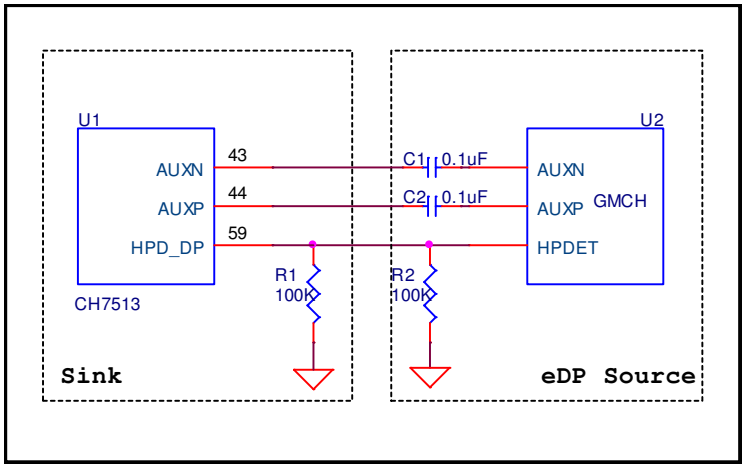
Figure 5: CH7513 DP Main Link Lane Inputs

• AUXP and AUXN

These two pins are for Display Port AUX channel control that accepts a half-duplex, bi-directional AC-coupled differential signal. An AC coupling capacitor, 0.1uF recommended, must be placed on the end as shown in **Figure 6**.

• HPDET

This output pin indicates whether the device is active or not. It also generates an interrupt pulse as defined by the Display Port standard. Output voltage is 3.3V. A resistor, greater than 100KΩ, should be connected between this pin and GND as shown in **Figure 6**.



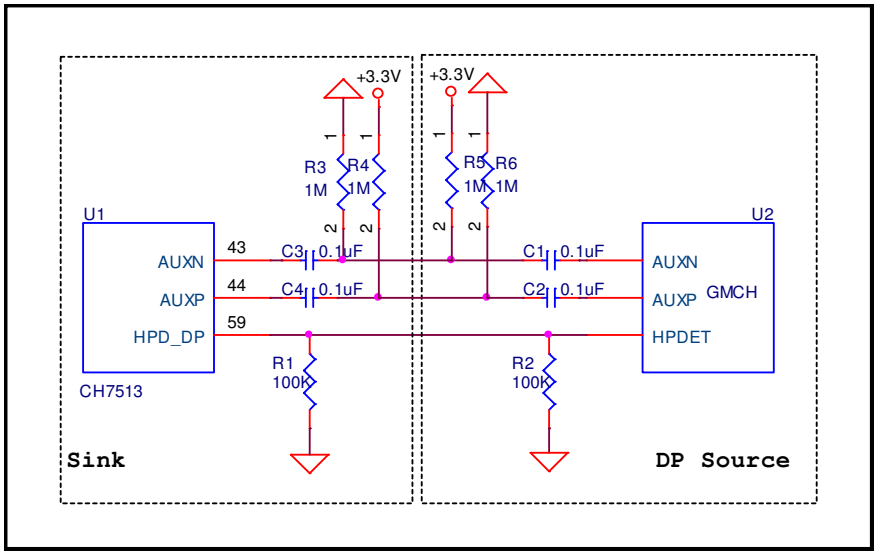


Figure 6: CH7513 AUX channel and HPDET

2.6 LVDS Signal Pins

• LVDS Outputs (LDCxP and LDCxN)

The LVDS output signals are LDCxP and LDCxN. The LVDS is a differential interface with a nominal swing 200mV. The following rules should be applied to the signals:

1. Keep traces as short as possible.
2. Make these traces have 100Ω differential impedance.
3. Trace widths should be 5 mils.
4. Intra Pair spacing (spacing between the "+" and "-" pairs) should be 7mils.
5. Inter Pair spacing (spacing between one differential pair and another) should be a minimum of 20 mils except in the area near the pins.
6. Difference in trace lengths between "+" and "-" pairs should be within 5mils.
7. Difference in trace lengths among Inter pairs should be within 10mils.
8. "+" And "-" pairs should be routed in parallel.

2.7 eDP bypass output

• eDP Pin Definition

CH7513 eDP main link and AUX pin definition follows COM express version 2.1.

Table 2: CH7513 Pin Assignments for the eDP bypass

eDP Signals	LVDS Signals	Alternative Pins
eDP_TX0P	RLV2P(PIN 26)	
eDP_TX0N	RLV2N(PIN 27)	
eDP_TX1P	RLV1P(PIN 28)	
eDP_TX1N	RLV1N(PIN 29)	
eDP_AUXP	RLVCLKP (PIN 24)(default)	SPC1(PIN 51)
eDP_AUXN	RLVCLKN (PIN 25) (default)	SPD1(PIN 50)
EDP_HPD	RLV0P(PIN 30)	EDP_HPD(PIN 2) (default)

By firmware default configuration, GPIO[0:3, 5] should be pulled high to light up the 4K2K eDP panel. For details please refer to the CH7513 Utility User Guide.

NOTE: If SPC1/SPD1 as eDP AUX CH, a switch chip (TS5A23166) need to avoid firmware loading fail as shown in **Figure 7**.

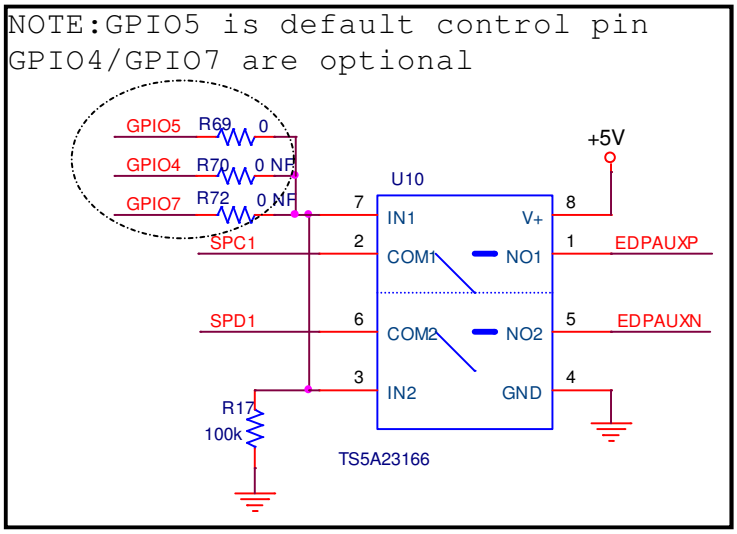


Figure 7: TS5A23166 Connection

2.8 Other function pins

• GLED, OLED

GLED and OLED pins output LED control signals to determine if the CH7513 is in normal or abnormal power and mode status. If GLED has output (3.3V), the CH7513 is in normal status. If OLED has output (flickers from 0 or 3.3V), the CH7513 is in abnormal status. The design is shown in **Figure 8**.

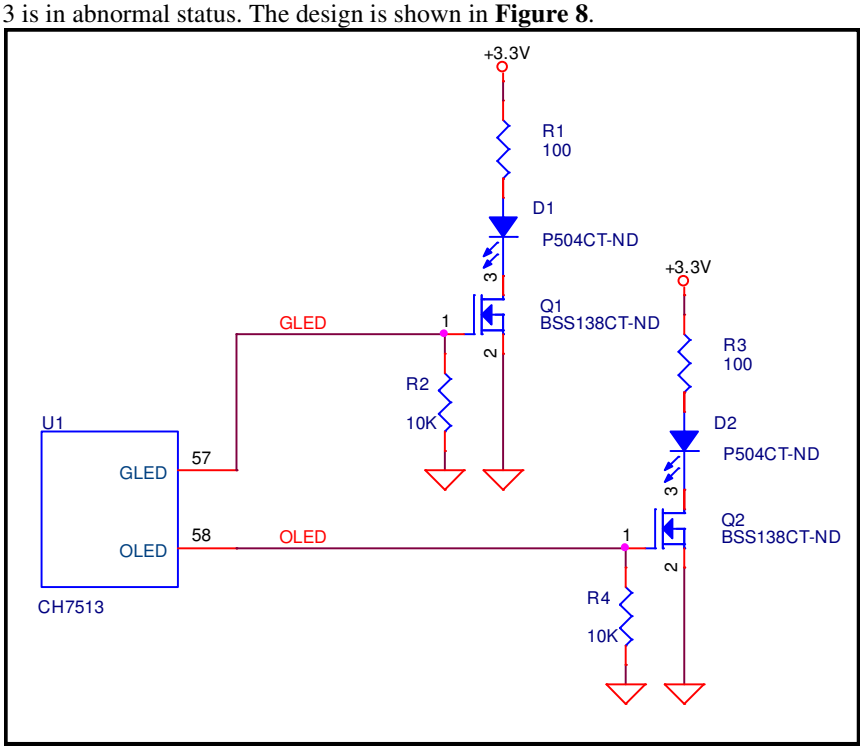


Figure 8: LED Control

• BLUP, BLDN

1. BLUP is the increase backlight brightness input pin.
2. BLDN is the decrease backlight brightness input pin.

Buttons can be placed at these pins to adjust the backlight brightness. The design is shown in **Figure 9**.

• PWRDN

The CH7513 enters into or exits power down state when receiving an active low pulse from this pin. The connection is shown in **Figure 9**.

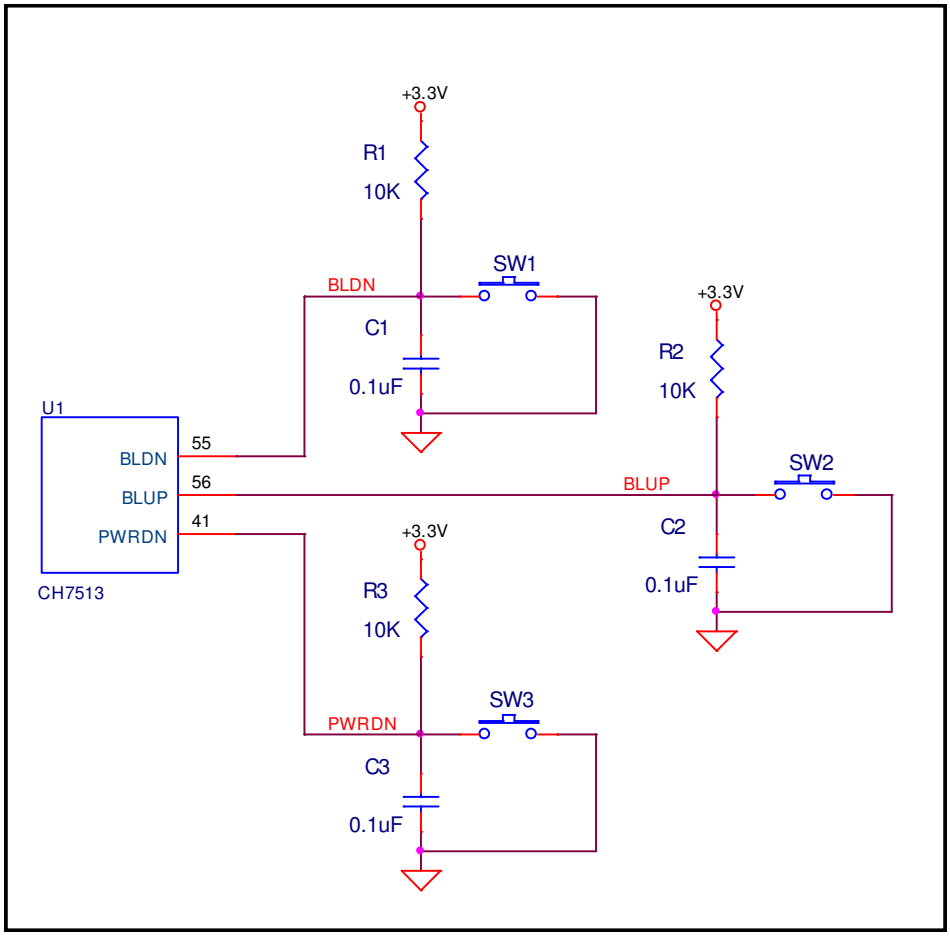


Figure 9: BLDN, BLUP and PWRDN Connections

• GPIO [0:3], GPIO [5]

These pins are general programmable IO pins. By firmware default configuration, These pins can be used as panel select signals. They can be pulled high or low forming into 16 different combinations. Every combination can match with one panel type. The connection is shown in **Figure 10**. CH7513 output mode and resolution can be controlled by GPIO[0:3, 5]. The detail please refer to CH7513 Utility User Guide.

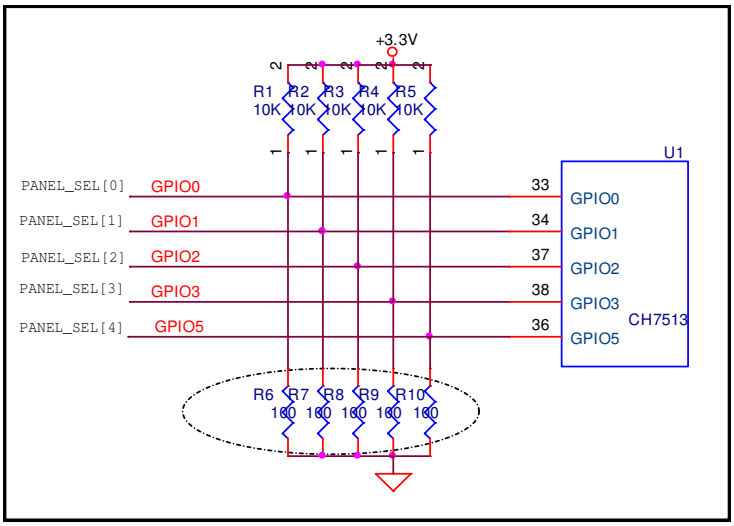


Figure 10: GPIO[0:3], GPIO[5] connections

Method 1 (default)

PANEL_SEL[4:0] can be connected to high (3.3V) or low (GND) level in CH7513 PCB board, CH7513 can get correct LVDS Panel selection value upon power ON.

Method 2

PANEL_SEL[4:0] can be controlled by other chip's GPIO pins in CH7513 application system. If the chip controlling CH7513 PANEL_SEL[4:0] cannot set expected value before CH7513 finishes loading its firmware (typically 100ms after CH7513 power ON), then the controlling chip can impose an active low pulse to CH7513 RB pin to restart EEPROM loading. It is recommended to reset CH7513 by the controlling chip each time LVDS Panel selection value is changed. The following figure shows the typical cases to control CH7513 PANEL_SEL[4:0] by other chip.

Figure 10 shows the typical cases to control the CH7513 PANEL_SEL[4:0] by another chip. Case 1 is the right loading case, in which the GPIO pins remains stable within 100ms after reset. Case 2 is the wrong loading case, in which the GPIO value, represented by the GPIO pins, is still at random after the firmware is completely loaded. Therefore, the reset signal must be given again. The reset pulse width of larger than 10ms is recommended.

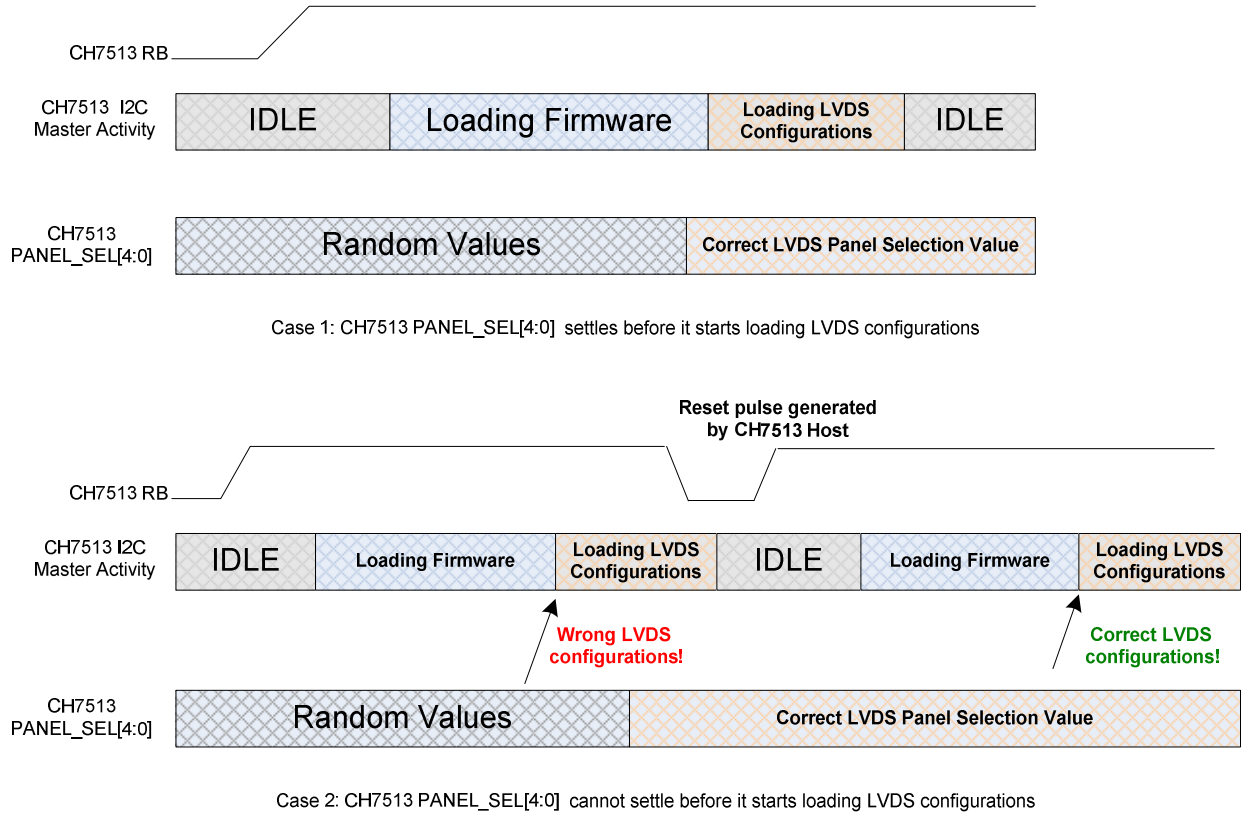


Figure 11: Typical cases to control CH7513 PANEL_SEL[4:0] by host chip

Note:

1. **The GPIO pins must remain stable for its corresponding value within 100ms after reset. Otherwise, a reset signal must be given again.**
2. **The firmware loading must be completed before VBIOS starts to function. Otherwise, some BIOS images may be lost.**

• PWM_OUT0, PWM_OUT1

The output Frequency from PWM_OUT0 can be up to 400 KHz. Its duty cycle ranges from 0% to 100%. Alternatively, the PWM bypass mode may be used to output the PWM signal through this pin. The voltage level is 3.3V.

The output Frequency from PWM_OUT1 can be up to 400 KHz. Its duty cycle ranges from 30% to 100%. The voltage level is 3.3V.

PWM_OUT0 and PWM_OUT1shall not be used at the same time. Customers may choose PWM_OUT0 or PWM_OUT1 in their application. Refer to the datasheet for detailed information.

• PWM_IN

PWM_IN has two working modes: Bypass mode and Duty Cycle Multiplication with AUX CH mode. In bypass mode, the input frequency to PWM_IN can be up to 1MHz. In Duty Cycle Multiplication with the AUX CH mode, the input frequency to PWM_IN can be up to 50 KHz. In either mode, the voltage level is 3.3V.

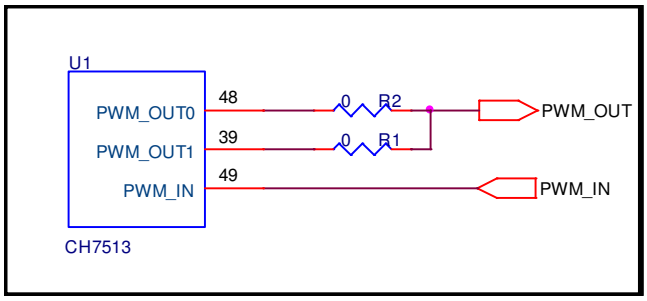


Figure 12: PWM Control connections

2.9 Important Design Considerations

(Panel power, backlight power, pull-up voltage)

• LVDS Power

Close attention must be paid to the power supplied to the LVDS backlight and the LVDS panel. Power requirements may differ from panel to panel. Please check the panels' power and backlight voltage specifications. The ENABKL and ENAVDD may be used to control the power for the LVDS backlight and the LVDS logic circuitry.

• Signal Wires, POWER and GND layout

Do not layout the wire or VIAs between the exposed thermal pad and the pin pads. Refer to **Figure 13**.

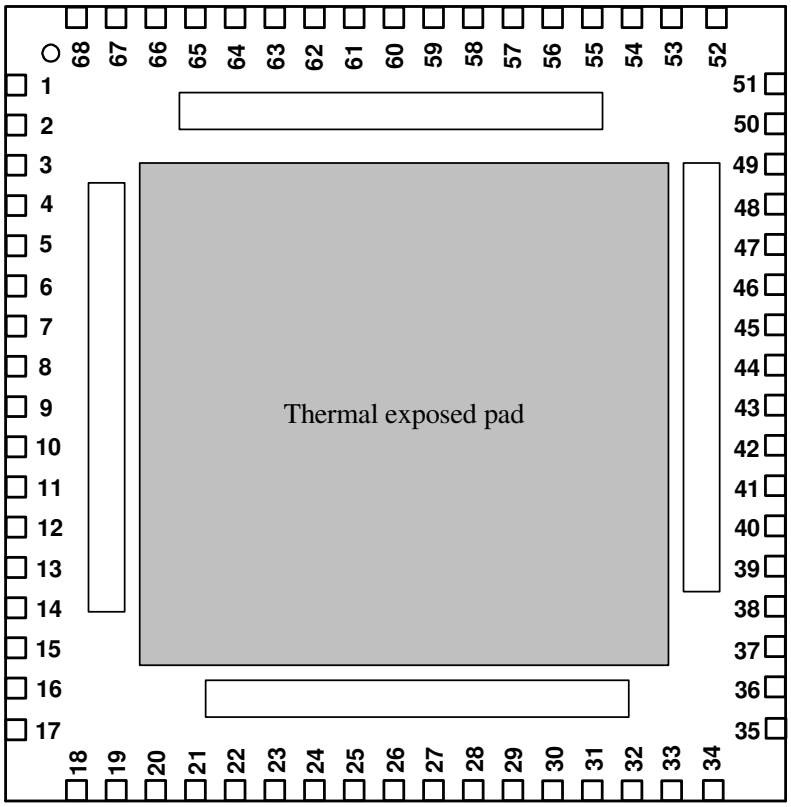


Figure 13: Wires or vias are not allowed in these four areas

2.10 Thermal Exposed Pad Package

The CH7513 is available in a 68-pin QFN package with exposed thermal pad. The advantage of the exposed thermal pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed thermal pad package provides a means of reducing the thermal resistance of the CH7513. Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed thermal pad of the package should be soldered to the PCB as shown in **Figure 14**.

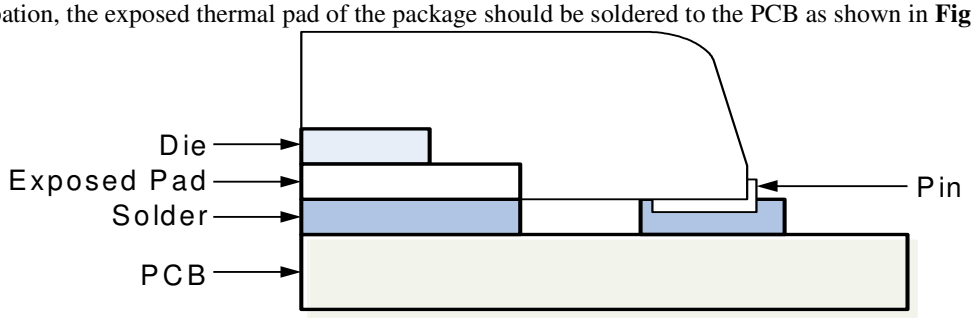


Figure 14: Cross-section of exposed thermal pad package

3.0 REVISION HISTORY

Table 3: Revisions

Rev. #	Date	Section	Description
0.1	08/19/2020	All	Layout Guide and Design Guide for CH7513 release.
0.2	03/18/2021	2.7 2.8	Add eDP bypass(4K2K) description.
0.3	06/07/2021	2.7	Add eDP bypass Alternative Pins
0.4	04/03/2023	2.1,2.3	Correct the power sequence and add more description about reset signal
0.5	04/25/2023	2.1	Correct the description about power sequence and reset signal

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